CLAIMS

What is claimed is:

1. An integrated circuit fabricated on a chip, comprising:

an on-chip logic analyzer including a word recognizer;

an on-chip memory capable of storing data selected by said word recognizer;

wherein said word recognizer includes a Boolean logic section and a counter/timer section located on-chip.

2. The system of claim 1, wherein the Boolean logic section includes a plurality of hardware match logical units which are capable of comparing a match value with internal state data, and which produce a true output signal if the comparison indicates a match condition.

3. The system of claim 1, wherein the Boolean logic section includes a plurality of hardware match logical units which are capable of comparing each bit of a match value with each bit of an internal state data signal, and which produce a true output signal for all bits if the comparison indicates a match.

4. The system of claim 3, wherein the hardware match logical units are capable of receiving a mask value, and wherein the hardware match logical units produce a true output signal for all bits that are masked.

5. The system of claim 4, wherein the hardware match logical units produce a single bit output signal that is asserted as true if a true output signal is obtained for all bits.

6. The system of claim 2, wherein the Boolean logic section further includes a plurality of software match logical units which are capable of detecting a software event, and which produce a true output signal if the event is detected.

7. The system of claim 6, wherein the Boolean logic section permits a user to selectively enable one or more individual hardware match logical units or software match logical units.

8. The system of claim 7, wherein the output signals of the hardware match logical units and the software match logical units connect to both an AND term and an OR term, and the user selects on an individual basis whether the AND term or the OR term will be enabled for each of the logical units.

9. The system of claim 8, wherein the logical units for which the AND term is selected have their output signals combined together in an AND gate, and all the logical units for which the OR term is selected have their output signals combined together in an OR gate.

10. The system of claim 9, wherein the output of the AND gate and the output of the OR gate may be selectively combined together in one of either an AND operation, an OR operation, a NAND operation, or a NOR operation.

11. The system of claim 10, wherein the output of the AND gate and the output of the OR gate are selectively combined in a multiplexer.

12. The system of claim 10, wherein the multiplexer output is selectively coupled to a second multiplexer via two different signal paths, and wherein the first signal path remains asserted if a match condition exists, and the second signal path is asserted for the first clock period that the match condition exists.

13. The system of claim 12, wherein the second multiplexer selects one of the first or second signal path based on a select bit that is programmed by the user.

14. The system of claim 2, wherein the counter/timer section comprises a counting device that is capable of being programmed by a user to count the number of times a match condition occurs, or the number of clock cycles during which a match exists.

15. The system of claim 14, wherein the counting device is loaded with a first initial value, and which is loaded with a second reload value if the counting device completes the count of the first initial value.

16. The system of claim 15, wherein the counting device comprises an incrementer.

17. The system of claim 15, wherein the counting device is reloaded with the first initial value if the counting device receives a load signal and the first initial value has not been satisfied.

18. The system of claim 17, wherein the load signal determines if the counting device will count a cumulative number of clock cycles during which a match exists, or a consecutive number of clock cycles that the match exists.

19. The system of claim 17, wherein the load signal determines if the counting device will count a cumulative number of clock cycles during which a match exists, or a consecutive number of clock cycles that the match exists.

20. The system of claim 15, wherein the counter/timer issues a Match signal when either the initial count value is satisfied or the second reload value is satisfied.

21. The system of claim 20, wherein the on-chip memory stores internal state data in response to the issuance of the Match signal.

22. The system of claim 21, wherein the on-chip memory comprises cache memory.

23. A processor, comprising:

an on-chip logic analyzer including a word recognizer;

an on-chip memory capable of storing data selected by said word recognizer;

wherein said word recognizer includes:

a Boolean logic section comprising a plurality of hardware match logical units that are capable of comparing a match value with internal state data, and which produce a true output signal if the comparison indicates a match condition; and

a counting device that is capable of being programmed by a user to count the number of times a match condition occurs, or the number of clock cycles during which a match condition exists.

24. The processor of claim 23, wherein the counting device is loaded with a first initial value from a first configuration and status register, and is subsequently reloaded with a second reload value from a second configuration and status register if the counting device completes the count of the first initial value.

25. The processor of claim 24, wherein the counting device comprises an incrementer.

26. The processor of claim 24, wherein the counting device is reloaded with the first initial value if the counting device receives a load signal and the first initial value has not been satisfied.

27. The processor of claim 26, wherein the load signal determines if the counting device will count a cumulative number of clock cycles during which a match exists, or a consecutive number of clock cycles that the match exists, and wherein the status of the load signal is controlled by a value programmed by the user in said first configuration and status register.

28. The processor of claim 26, wherein the load signal determines if the counting device will count a cumulative number of clock cycles during which a match exists, or a consecutive number of clock cycles that the match exists.

29. The processor of claim 26, wherein the counter/timer issues a Match signal when either the initial count value is satisfied or the second reload value is satisfied, and in response to issuance of the Match signal, the on-chip memory stores internal state data.

30. The processor of claim 26, wherein the expiration of the initial count value causes said memory device to begin storing internal state data, based on an interval defined by the reload count value.

31. The processor of claim 23, wherein the Boolean logic section further includes a plurality of software match logical units which are capable of detecting a software event, and which produce a true output signal if the event is detected.

32. The processor of claim 31, wherein the Boolean logic section permits a user to selectively enable one or more individual hardware match logical units or software match logical units.

33. The processor of claim 32, wherein the output signals of the hardware match logical units and the software match logical units connect to both an AND term and an OR term, and the user selects on an individual basis whether the AND term or the OR term will be enabled for each of the logical units.

34. The processor of claim 33, wherein the logical units for which the AND term is selected have their output signals combined together in an AND gate, and all the logical units for which the OR term is selected have their output signals combined together in an OR gate.

35. The processor of claim 34, wherein the output of the AND gate and the output of the OR gate may be selectively combined together in one of either an AND operation, an OR operation, a NAND operation, or a NOR operation.

36. The processor of claim 35, wherein the output of the AND gate and the output of the OR gate are selectively combined in a multiplexer.

37. A processor fabricated on a chip, comprising:

an on-chip logic analyzer including a word recognizer;

an on-chip memory capable of storing data selected by said word recognizer;

wherein said word recognizer includes:

a Boolean logic section comprising one or more hardware match logical units that are capable of comparing a match value with internal state data, and which produce a true output signal if the comparison indicates a match condition, and one or more software match logical units which are capable of detecting a software event, and which produce a true output signal if the event is detected.

38. The processor of claim 37, further comprising a counting device that is capable of being programmed by a user to count the number of times a match condition occurs, or the number of clock cycles during which a match condition exists or an event has been detected.

39. The processor of claim 37, wherein the Boolean logic section permits a user to selectively enable one or more individual hardware match logical units or software match logical units.

40. The processor of claim 39, wherein the output signals of the hardware match logical units and the software match logical units connect to both an AND term and an OR term, and the user selects on an individual basis whether the AND term or the OR term will be enabled for each of the logical units.

41. The processor of claim 40, wherein the logical units for which the AND term is selected have their output signals combined together in an AND gate, and all the logical units for which the OR term is selected have their output signals combined together in an OR gate.

42. The processor of claim 41, wherein the output of the AND gate and the output of the OR gate may be selectively combined together in one of either an AND operation, an OR operation, a NAND operation, or a NOR operation.

43. A word recognizer fabricated as part of an integrated circuit, comprising:

a Boolean logic section;

a counter/timer section; and

wherein said Boolean logic section and said counter/timer section are located on-chip.

44. The system of claim 43, wherein the Boolean logic section includes a plurality of hardware match logical units which are capable of comparing a match value with internal state data of the

integrated circuit, and which produce a true output signal if the comparison indicates a match condition.

45. The system of claim 43, wherein the Boolean logic section includes a plurality of hardware match logical units which are capable of comparing each bit of a match value with each bit of an internal state data signal, and which produce a true output signal for all bits if the comparison indicates a match.

46. The system of claim 45, wherein the hardware match logical units are capable of receiving a mask value, and wherein the hardware match logical units produce a true output signal for all bits that are masked.

47. The system of claim 46, wherein the hardware match logical units produce a single bit output signal that is asserted as true if a true output signal is obtained for all bits.

48. The system of claim 44, wherein the Boolean logic section further includes a plurality of software match logical units which are capable of detecting a software event, and which produce a true output signal if the event is detected.

49. The system of claim 48, wherein the Boolean logic section permits a user to selectively enable one or more individual hardware match logical units or software match logical units.

50. The system of claim 49, wherein the output signals of the hardware match logical units and the software match logical units connect to both an AND term and an OR term, and the user selects on an individual basis whether the AND term or the OR term will be enabled for each of the logical units.

51. The system of claim 50, wherein the logical units for which the AND term is selected have their output signals combined together in an AND gate, and all the logical units for which the OR term is selected have their output signals combined together in an OR gate.

52. The system of claim 51, wherein the output of the AND gate and the output of the OR gate may be selectively combined together in one of either an AND operation, an OR operation, a NAND operation, or a NOR operation.

53. The system of claim 52, wherein the output of the AND gate and the output of the OR gate are selectively combined in a multiplexer.

54. The system of claim 52, wherein the multiplexer output is selectively coupled to a second multiplexer via two different signal paths, and wherein the first signal path remains asserted if a match condition exists, and the second signal path is asserted for the first clock period that the match condition exists.

55. The system of claim 54, wherein the second multiplexer selects one of the first or second signal path based on a select bit that is programmed by the user.

56. The system of claim 44, wherein the counter/timer section comprises a counting device that is capable of being programmed by a user to count the number of times a match condition occurs, or the number of clock cycles during which a match exists.

57. The system of claim 56, wherein the counting device is loaded with a first initial value, and which is loaded with a second reload value if the counting device completes the count of the first initial value.

58. The system of claim 57, wherein the counting device comprises an incrementer.

59. The system of claim 57, wherein the counting device is reloaded with the first initial value if the counting device receives a load signal and the first initial value has not been satisfied.

60. The system of claim 59, wherein the load signal determines if the counting device will count a cumulative number of clock cycles during which a match exists, or a consecutive number of clock cycles that the match exists.

61. The system of claim 59, wherein the load signal determines if the counting device will count a cumulative number of clock cycles during which a match exists, or a consecutive number of clock cycles that the match exists.

62. The system of claim 57, wherein the counter/timer issues a Match signal when either the initial count value is satisfied or the second reload value is satisfied.

63. The system of claim 62, further comprising an on-chip memory that stores internal state data in response to the issuance of the Match signal.

64. The system of claim 63, wherein the on-chip memory comprises cache memory.